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Ultra-Thin Chips with Printed Interconnects on Flexible Foils

*Sihang Ma, Yogeenth Kumaresan, Abhishek Singh Dahiya, and Ravinder Dahiya**

"Heterogeneous Integration" is a promising approach for high-performance hybrid flexible electronics that combine printed electronics and silicon technology. Despite significant progresses made by integrating rigid silicon chips on flexible substrates, the integration of flexible ultra-thin chips (UTCs) on flexible foils remains a challenge as they are too fragile for conventional bonding methods. Reliable interconnects (low-resistivity and mechanical robustness) and bonding of UTCs are critical to the realization of hybrid flexible systems. Herein, using a non-contact printing approach, an easy and cost-effective method for accessing UTCs on flexible foils is demonstrated. The high-viscosity conductive paste, extruded from a high-resolution printer (1–10 µm line width), is used here to connect the metal oxide semiconductor field effect transistors (MOSFETs) on UTCs with the extended pads on flexible printed circuit boards (PCBs). The electrical characterization of MOSFETs, before and after printing the interconnects, reveals an acceptable level of variation in device mobility (change from 780 to 630 $cm^2 V^{-1}s^{-1}$). This is due to the drop in effective drain bias voltage as a marginally small electrical resistance (≈30 Ω) is added by the printed interconnects. The bonded UTCs show robust device performance under bending conditions, indicating high reliability of both the chip thinning and bonding methods.

1. Introduction

Hybrid flexible electronic systems that combine printed electronics and silicon technology are being explored for applications such as wearables, soft robotics, ultra-thin displays, healthcare, etc. to meet the large area electronic requirements with high performance and low data latency.[1,2] It is difficult to have these attributes with current silicon technology or printed electronics alone. It is to an arduous task to realize the large area electronics with silicon technology alone and it is challenging to attain the high performance and low data latency with printed electronics alone.[2–5] Nonetheless, the latter has opened the "resource-efficient" and potentially greener routes for obtaining electronics on diverse substrates.[6] Therefore, putting together the devices developed using both the silicon technology and printed electronics, as hybrid systems, is a practical way forward. To this end, "flexible hybrid electronics (FHE)" or "heterogeneous integration" that combines conventional silicon chips or ultra-thin chips (UTCs) with printed devices is gaining significant interest.[7] Reliable interconnects are key to the realization of such hybrid high performance flexible electronic systems.

Due to considerable differences in mechanical and thermal requirements, it is challenging to use conventional bonding and interconnect technology to robustly connect the UTCs on flexible substrates with other printed devices. Conventional wire bonding approaches including thermocompression, thermosonic, and ultrasonic bonding introduce mechanical force (ranging from 0.2 to 1.5 N) during bonding processes.[8] Besides, thermocompression and thermosonic bonding processes require high temperature, 200–400 °C, whereas most of the polymeric flexible substrates become unstable at such high temperatures.[9] Traditional UTC interposer technologies such as Flip Chip (FC) assembly, UTC Package (UTCP), and Through Silicon Via (TSV) have also been widely explored.[10] Their common technological drawbacks involve the need for using MEMS fabrication equipment, pre-patterned masks, and chemical etching, all of which can increase the complexity and cost of the manufacturing process. Moreover, FC has limitations toward the application of chips, being inapplicable with devices facing up, such as pressure sensors.[11] UTCP is not ideal for heat dissipation as the device is embedded in two polymers.[5] TSV fabrication requires copper (Cu) but the thermal expansion coefficient of Cu mismatches with that of Si, which can result in wafer warpage.[12] Considering these difficulties, the printing route is considered here for gaining access to UTCs. With printing technologies, it is possible to deposit conductive materials for electrical connections at low temperatures. As a single-step additive approach, printing technologies are more straightforward and cost-effective than the conventional UTC interposers.

Driven by these motivations, we present here a non-contact printing approach to realise the reliable interconnects for flexible hybrid electronic systems. The high-viscosity Ag conductive paste (>100 000 cP, 82 wt% of metal), extruded from a high-resolution printer (1–10 µm line width), is used here to connect the metal oxide semiconductor field effect transistors (MOSFETs) on UTCs (35 ± 0.6 µm thick) with the extended pads on flexible printed circuit boards (PCBs). The MOSFETs showed no significant change in the performance after thinning, bonding, and bending. Unlike

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Table 1. Comparison between non-contact printing technologies.

Technologies	Printing resolution	Printing directions	Number of printing layers to cover a step height of >30 μm	Disadvantages	Ref.
Screen printing	50–100 μm	Horizontal	N/A	• Material waste including old screens, stencil waste, waste inks and screen reclamation chemicals	[4]
Inkjet printing	20–50 μm	Horizontal and vertical	≈20–100 layers (line thickness = ≈0.3–1.5 μm)	• Ink spreading affecting the resolution, morphology of the printed patterns, integration degree and eventually the electrical stability of the printed electronics • Discrete drop nature causing droplet bulging, scalloping or even open lines • Surface treatment needed through photolithography	[17,18]
Aerosol jet printing (AJP)	10 μm	Horizontal and vertical	6–15 layers (line thickness = ≈2–5 μm)	• Discontinuity in line morphology • Degraded performance from overspray	[16,19]
Laser direct write (LDW)	10 μm	Horizontal	N/A	• Unable to print on organic substrates • Only available for flat substrates	[20]
Extrusion printing	≈1 μm	Horizontal and vertical	1 layer	• Optimization required	This work

contact based printing methods such as offset lithography, gravure printing and flexography,[4] the presented approach does not involve direct contacts between the printing tool and the substrate. In doing so, we have prevented the application of mechanical stress and hence the breakage of physically fragile UTCs. Inkjet printing is another non-contact method that has been explored for realizing interconnects on flexible substrates. However, it is impractical to use inkjet printing to secure connections with the pads of UTCs as this will require multiple layers of printing (≈20–100 layers) to attain a typical step height of >30 μm. Further, the interconnect resolution plays a significant role as many high-performance electronic devices nowadays require bond pads with ultra-fine pitches (<50 μm), narrow tracks (<10 μm) and some interconnect heights (<60 μm).[13] Such features are currently difficult to achieve as the aqueous fluids on substrates typically acquire two to four times larger size than the droplet from the nozzle.[14] In this regard, aerosol jet printing (AJP), laser direct write (LDW), and extrusion of high-viscosity conductive paste stand out.[15] However, similar to inkjet printing, AJP also requires multi-layer printing to obtain vertical structures.[16] LDW does not support vertical printing and is not compatible with different materials and flexible plastic substrates. **Table 1** shows the comparison between non-contact printing technologies regarding their printing resolution, capability of printing directions, and disadvantages.

The paper is organized as follows: Section 2 presents processes of realizing the interconnects and bonding on ultra-thin MOSFET chips. Section 3 presents the device characterization before and after thinning, bonding, and bending. Key outcomes are summarized in Section 4.

2. Experimental Section

2.1. Thinning

A silicon chip with a matrix of 4 × 4 MOSFET devices was used in this study to demonstrate the reliable bonding of UTCs on flexible substrate. The chip thinning steps are described in detail in the previous paper and shown in **Figure 1**a.[21] Briefly, the process started by thinning a bulk Si chip with thickness ≈520 μm (Figure 1a(i)). To achieve mechanical flexibility, backside lapping process assisted with polymethyl methacrylate (PMMA) sacrificial technique was utilized for thinning the MOSFET chip. In the previous work, the importance of PMMA sacrificial layer was presented during the process of separating the UTC from the sample holder after thinning.[21] Without such technique, the thinned chip (<50 μm thickness) was highly prone to breakage during the separation process. Therefore, in this work, a similar approach has been followed. Prior to thinning, the device side of the chip was spin coated with a ≈20 μm-thick PMMA sacrificial protection layer (Figure 1a(ii)), followed by firmly attaching to a sample holder via low-stress wax. Subsequently, the sample was firmly placed onto the Logitech lapping jig through vacuum, which was then connected to the lapping machine (Figure 1a(iii)). As a result of thinning, the thickness of the MOSFET chip was reduced from ≈520 to 35 ± 0.6 μm (Figure 1b). Next, the sample was detached from the sample holder and the PMMA sacrificial layer was removed using acetone solution.

2.2. Bonding by Printing

Prior to bonding by printing, the ultra-thin MOSFET chip was attached to a flexible printed circuit board (PCB) via a small amount of the low-stress adhesive, EpoTEK 301-2 (Figure 1c(i)). The electrical interconnects in this work were formed using a high-resolution non-contact extrusion printer (Delta printer by XTPL), as shown in Figure 1c. Firstly, the nozzle opening size and ink material were selected considering the resolution and conductivity of the printed structures. The available nozzle opening sizes were 1.5, 3.5, and 5 μm diameters, which directly affect the printing resolution. An ≈1 μm feature size can be achieved as the highest resolution for the extrusion printing system, as mentioned in Table 1. However, in the case of utilizing printing techniques for UTC bonding, robustness and

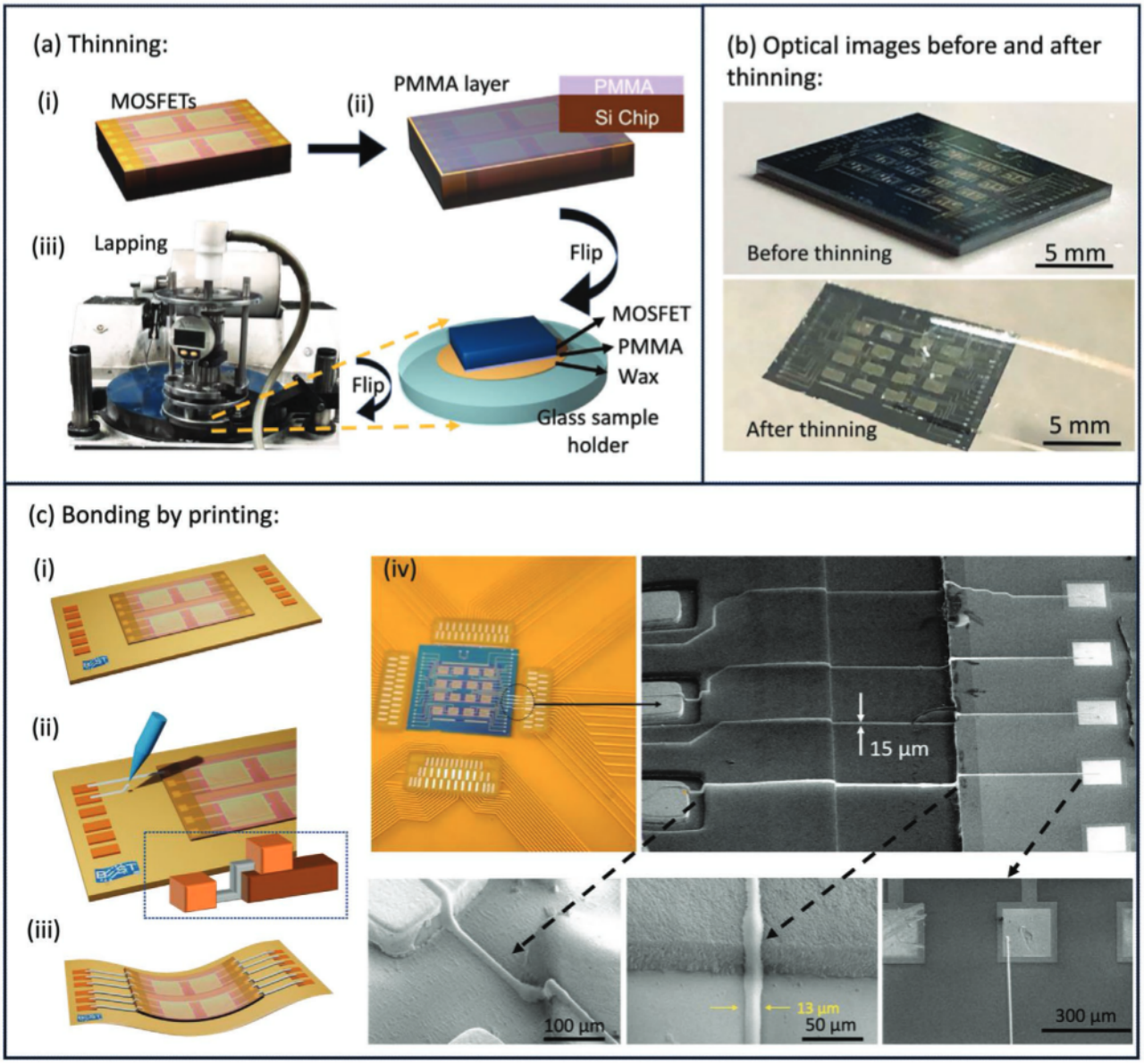

Figure 1. Schematics of realising the ultra-thin MOSFET chip: a) Thinning: (i) MOSFET chip with an original thickness of ≈520 µm, (ii) MOSFET chip spin coated with ≈20 µm PMMA sacrificial layer with a cross-section scheme (inset); (iii) Sample attached on a glass sample holder through wax with the device side facing down mounted onto the lapping jig for chip thinning through a lapping machine; b) Optical images of the bulk MOSFET chip and UTC; c) Bonding by printing: (i) Thinned chip attached on flexible PCB; (ii) Interconnects between the chip and flexible PCB realized by the non-contact extrusion printing of high-viscosity ink with a cross-section scheme (inset); (iii) scheme of realized flexible ultra-thin MOSFET chip; (iv) Optical and SEM images of ultra-thin MOSFET chip attached on the flexible PCB with printed interconnects.

conductivity also need to be taken into consideration. To meet such criteria, interconnects with relatively larger features were required to lower the resistance. It was easier to achieve this with a bigger nozzle size and hence a nozzle with the 5 µm opening size was used in this work. The choice of ink also plays a significant part in the performance of the bonding structure as low viscosity ink can spread on the substrate and lead to unstable electrical performance or even short circuiting of pads. For UTC bonding, uniform and continuous printed conductive track was needed to connect the MOSFET chip with flexible PCBs. As there was a step of 35 ± 0.6 µm between the chip and PCB, inks with a high viscosity were preferred. Accordingly, silver (Ag) nano-paste, XTPL CL85, with spherical Ag nanoparticles (35–50 nm diameter and 82 wt% of metal) was used with the viscosity above 100 000 cP (measured at room temperature with a shear rate of 0.2 s^{-1}). Ag as the chip bonding material has been widely explored because of its inherent properties such as high electrical conductivity, high thermal conductivity and high melting point.[22] The metal content of CL85 was more than that of commercially available inks by 20 wt% (NPS-J from Harima, metal content: 62–67%).[23] Compared with the counterparts for other printing technologies such

as direct ink write (DIW), inkjet, electrohydrodynamic inkjet (EHD), etc., the paste viscosity in this work is also the highest so far (ink viscosity of DIW: < 1000 cP, inkjet: <40 cP, electrohydrodynamic: <10 000 cP).[18,24] Considering the rheology for different ink/paste for printing technologies, they usually exhibit non-Newtonian behavior, which means that their effective viscosity does not remain constant and depends on the shear rate. In the case of all printing inks or paste, the viscosity decreases as the nozzle diameter becomes smaller toward the tip and the shear rate increases due to the influence of shear thinning. Therefore, the effective viscosity at the nozzle tip was orders of magnitude smaller. However, based on the thixotropic behaviour, the viscosity of the ink or paste deposited on the substrate after printing can return to the initial viscous state. As a result, despite the wettability of the substrate, continuous electrical connections with high aspect ratio can be achieved with high-viscosity materials. The XTPL printer employed here is simple to use as it requires optimization of two parameters (pressure and velocity of 8 bars and 0.02 mm s^{-1} used in this work) only. Following the optimization of printing conditions, the conductive Ag interconnects were formed to connect the thinned MOSFET chip with the metal lines on flexible PCBs. As required by the design of the sample with a step height between pads on the chip and those on the PCB, the printing angle between the nozzle and substrate was set to be 75°. To cover the step height of the thinned chip, the nozzle was simply shifted gradually along the Z-axis. At last, the conductivity of the printed structures was improved by performing annealing at 150 °C for 15 min.

2.3. Electrical Characterization

Electrical characterizations of the thinned MOSFET UTCs, bonded on flexible PCBs, were performed in an ambient and dark environment using Cascade Micro-tech Auto-guard probe station interfaced to a semiconductor parameter analyser (B1500A, Agilent).

3. Results and Discussion

3.1. Evaluation of the Chip before Printing Interconnects

To monitor the effect of chip thinning, the transfer and output characteristics of the MOSFET device were obtained before and after thinning under similar conditions. To obtain the transfer (I_d–V_g) scans, the gate-source voltage (V_g) was swept from –0.5 to +1.75 V at drain bias (V_d) of 0.3 and 0.5 V (**Figure 2**a). The family of output (I_d–V_d) scans were obtained by sweeping V_d from 0 to 1.75 V and V_g was incrementally stepped from 0 to 1.5 V with a step of 0.5 V after a full sweep of V_d (Figure 2b). From the output and transfer data, increasing V_g toward more positive values resulted in an increase of the drain current (I_d). This is typical of an n-channel MOSFET operation. Notably, the low-V_d region in the output scans ($V_d \leq \approx 0.1$ V) shows a linear dependence of I_d with increasing V_d without any inflection point. This behaviour of the device is typical of a MOSFET operating in the linear regime with low energetic contact barriers. A clear I_d saturation with an increasing V_d was observed, showing excellent gate control over the semiconducting channel. The device characterization before and after thinning presents negligible changes, as can be seen from Figure 2a,b. A quantitative comparison for key MOSFET performance parameters such as mobility, current on/off ratio, etc. is also made for before and after chip thinning and discussed in the next section and summarized in **Table 2**.

Thinning of Si chips can damage the interface quality (semiconductor/oxide and oxide/bulk) of the MOSFET. The gate bias stress is believed to be the critical characteristic to understand the interface quality of the MOSFET after the thinning process and the presence of defects could lead to a time-dependent threshold voltage shift.[25] For n-channel MOSFETs and/or n-type thin film transistors, an increase in the positive bias stress (PBS) tends to attract more electrons toward the interface between the channel and the dielectric layer. These electrons are trapped either at low energy level or deep energy level trap states created by oxygen vacancy and oxygen interstitial defects of dielectric at the channel/dielectric interface. The electrons trapped at low energy levels are released back to the channel immediately, but the ones trapped at higher energy levels require more time, which results in a decrease in the number of carriers in the channel and simultaneously affects the key parameters of the MOSFET. To understand the channel/dielectric interface quality after thinning, the PBS was performed by applying a 2 V gate bias and 0.5 V drain bias for 2000 s and sequentially the transfer characteristics were measured at a regular interval, as shown in Figure 2c. Further, the key parameters such as threshold voltage and subthreshold swing (SS) values were extracted from the transfer curve. The extracted values are plotted and displayed in Figure 2d. Interestingly the key parameters of the device remain constant over 2000 s, which confirms that the dielectric/channel interface quality is not affected by the thinning process. Similarly, a negative bias stress was performed by applying a negative gate bias of –2 V for 2000 s and the transfer characteristics at the same intervals were measured, as shown in Figure 2e. The SS values were extracted using the logarithmic transfer curve plot (Figure S1, Supporting Information). Under negative bias stress, a slight positive shift in the threshold voltage value was observed. In general, the positive shift in the threshold voltage of n-channel MOSFET is observed due to the body effect when the source terminal and the body terminal are at different bias as per Equation (1):

$$V_T = V_{To} + \gamma\left[\left(2|\phi_F| - V_{BS}\right)^{1/2} - \left(2|\phi_F|\right)^{1/2}\right] \quad (1)$$

where γ is the body bias coefficient, $|\phi_F|$ is the Fermi potential of the material and the V_{BS} is the voltage difference between the source and the body terminal. The threshold voltage (V_T) shift takes places when there is a non-zero V_{BS} value. In other words, the difference in the source voltage and the body voltage results in a shift in the threshold voltage. In our case, the source and body terminal of our n-channel MOSFETs are connected to each other. This eliminates the possibility of threshold voltage shift due to the body effect. In the case of metal oxide-based thin film transistors, a negative shift in threshold voltage is observed under the negative bias stress due to the interaction of the back-channel surface with moisture and/or traps.[2] In

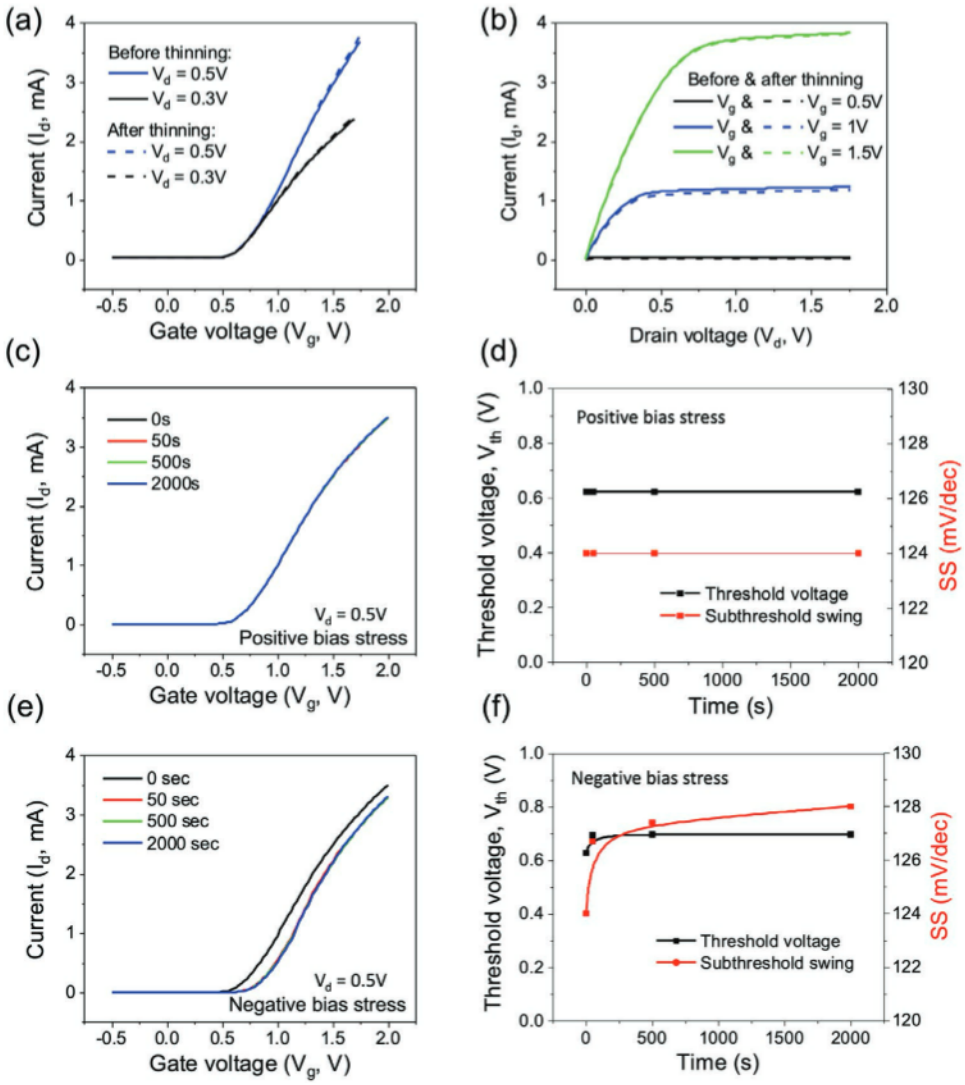

Figure 2. Device characterization results: a) Transfer function before and after thinning; b) Output function before and after thinning; c) Positive bias stress study after thinning at V_d = 0.5 V; d) Threshold (in black) and subthreshold (in red) values extracted from PBS; e) Negative bias stress study after thinning V_d = 0.5V; f) Threshold (in black) and subthreshold (in red) values extracted from NBS.

the current MOSFET, the constant negative bias on the gate terminal tends to deplete the free electrons from the channel at the channel/dielectric interface. Thereby, the number of electrons near the channel/dielectric interface region is decreased. Hence, higher positive gate bias is required to achieve a charge accumulation between the source and drain, which results in the positive shift in the threshold voltage as shown in Figure 2f. However, the observed shift in threshold voltage is very small (≈0.1 V) and reversible.

The difference in the device field-effect mobility (μ_{FE}) before and after thinning is also studied. Firstly, V_T was extracted using the linear extrapolation method. For this, the linear

Table 2. Comparison of MOSFET key parameters under different conditions.

Condition	Peak mobility [$cm^2 V^{-1}s^{-1}$]	Peak transconductance (g_m) [mS]	V_t [V]	S-S [mV dec^{-1}]	Current on/off ratio
Before thinning	780	2.6	0.6	≈125	$>10^4$
After thinning	720	2.6	0.6	≈125	$>10^4$
After bonding	630	2.1	0.6	≈125	$>10^4$
Bending after thinning	750	2.5	0.6	≈125	$>10^4$
Bending after bonding	630	2.1	0.6	≈125	$>10^4$

extrapolation of I_d–V_g in excepting the $I_d = 0$ axis gives the V_T value. This is followed by the calculation of g_m, according to Equation (2) shown below:

$$g_m = \frac{\partial I_d}{\partial V_g} | V_d = \text{constant} \quad (2)$$

The extracted parameters are used to calculate the field-effect mobility, μ_{FE}, using Equation (3) where W and L are the gate width and length respectively and C_{OX} stands for the oxide capacitance (W/L = 2000 µm/12 µm, thickness of silicon dioxide (SiO_2) = 50 nm in this work).

$$\mu_{FE} = \frac{g_m}{C_{ox}\left(\frac{W}{L}\right)V_d} \quad (3)$$

The mobility and threshold voltage before and after thinning remain unchanged, 780 $cm^2\ Vs^{-1}$ and 0.6 V respectively showing that the lapping with PMMA sacrificial technique is reliable for UTC thinning and does not affect the device performance. Also, other important MOSFET performance-defining parameters stay constant, as shown in Table 2.

3.2. Evaluation of the Chip after Printing Interconnects

We also investigated the device performance after realizing the interconnects by printing. Transfer (**Figure** 3a) and output (Figure 3b) scans were performed under similar conditions as prior to thinning and bonding the MOSFET chip.

The measurements were performed by placing the electrical probes on peripheral or extended contact pads on the flexible PCB. The mobility value was extracted from the transfer characteristics using Equation (3). The extracted mobility values before and after bonding are shown in Figure 3c. Compared with the characterization results after thinning, the device performance demonstrated a minor decrease in drain current (transconductance) which resulted in the reduction of carrier mobility ($\mu_{FE} \approx$ 630 $cm^2\ Vs^{-1}$ after bonding) although other device parameters such as threshold voltage, SS, etc. remain unchanged (Figure 3d). The decrease in mobility after printing the interconnects is explained as follows:

An equivalent circuit for a bonded MOSFET device is shown in Figure S2 (Supporting Information). Two additional resistances (R1 and R2) connected in series are added to the MOSFET channel after printing interconnects. The value of these extra resistors plays a significant role in defining the transconductance of the device and thus, the field effect mobility. Accordingly, the electrical characterization of the printed structured was first evaluated. The resistivities of each connection from MOSFET channels (drain, gate, and source) on the chip pads to the PCB pads were measured. Results were ≈4.2 × 10^{-8} Ωm, equivalent to the conductivity of 40% bulk Ag, revealing the highest conductivity in comparison with conventional interconnect materials such as Cu/low-k, carbon nanotube (CNT) and graphene nanoribbon (GNR).[26] Nevertheless, the additional

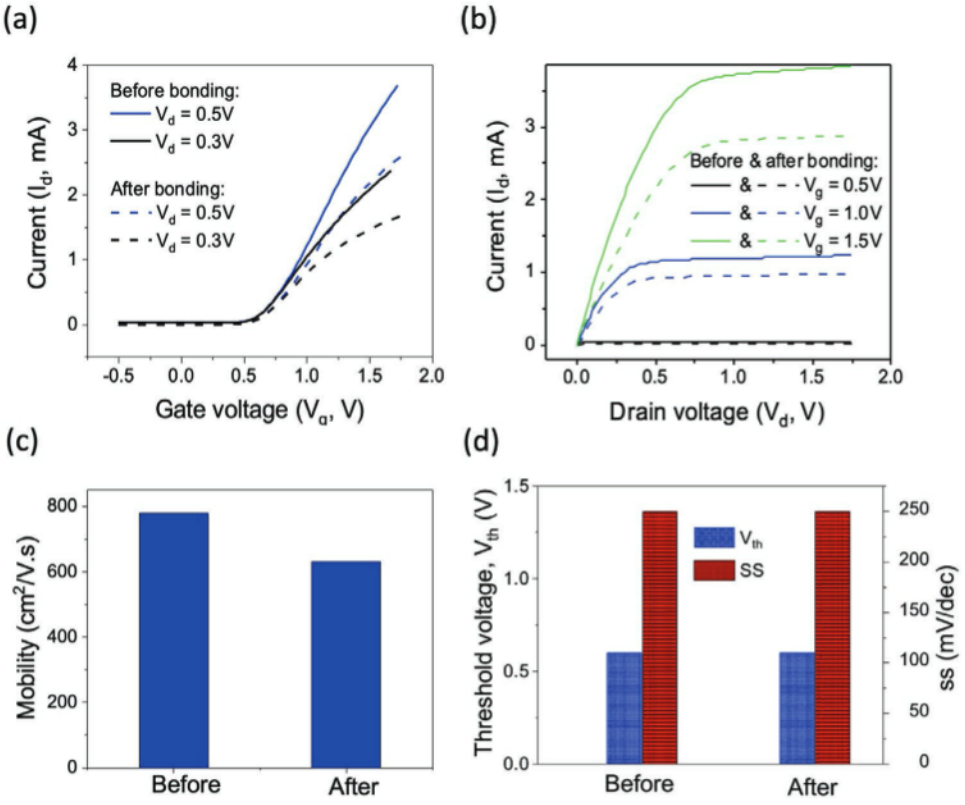

Figure 3. Device characterization before and after bonding by printing: a) Transfer functions; b) Output functions; c) Mobility; d) Threshold and sub-threshold voltages.

resistance (≈30 Ω each) in series leads to small voltage drop across them and thus reduced the effective drain bias across the MOSFET channel. Based on the measured resistance of printed bonding lines, we have theoretically calculated the voltage drops on each resistor load when connected in series and summarized in Table S1 (Supporting Information). Accordingly, such a decrease in mobility could potentially originate from the additional resistance between the chip pads to the PCB pads generated by the printed structures.

In addition, the device flexibility was studied by placing the thinned chip on a 3D printed concave test rig with a radius curvature of 40 mm (Figure S3, Supporting Information) where the thinned MOSFET experienced compressive uniaxial bending stress. Firstly, the bending effect was studied and compared under planar and bending after thinning of chips. In this case the characterization was carried out directly on the chip pads. As can be seen from the characterization results on **Figure 4**a,b, a slight decrease in the drain current, I_d, was observed under the compressive stress. This is attributed to the variation in the band structure. The conduction band is split into two subbands, Δ_2 and Δ_4, under uniaxial strain due to the quantum confinement effects.[27] Meanwhile, the intensity of the transverse electric field changes the energy difference between $\Delta_2$and Δ_4, causing the bandgap to shift. As a result, with an increase of compressive strain, more electrons occupy the Δ_4 valleys, causing more effective mass in Δ_4.[28] Additionally, the carrier transport in MOSFETs is also affected by the interface scattering at the Si/SiO_2 interface, which increases with the transverse electric field.[2,29] Consequently, there is a reduction in total gate capacitance and a rise in resistance under compressive stress, which leads to a decrease in mobility.[30] As the change in mobility is in relation with that of the drain current, as expressed in Equation (4) where Π is the piezoresistive coefficient and σ is the conductivity, the output current decreases in our study.[31]

$$\frac{\Delta I_d}{I_d} = \frac{\Delta \mu}{\mu} = \Pi \sigma \tag{4}$$

Meanwhile, the extracted mobility under bending after thinning (750 $cm^2\ V^{-1}s^{-1}$) is 30 $cm^2\ V^{-1}s^{-1}$ lower than under the planer condition (780 $cm^2\ V^{-1}s^{-1}$) without the V_T being shifted.

The bending tests were conducted after forming interconnects under similar conditions. Interestingly, the drain current showed a slightly higher value under concave bending than under planar condition after bonding by printing whereas a decrease in the device on-current was observed under convex bending (Figure 4c,d). This can be explained as follows: While the UTC was under +0 mm concave bending condition, the printed conductive track also experienced the compressive stress, as a result of which the Ag nanoparticles became more compact and the contact area between Ag particles was improved.[32] As previously mentioned, our Ag nano-paste has high metal content (82 wt% Ag nanoparticles) and conductivity compared with conventional printing or interconnect materials. Thanks to the high metal content of Ag, the resistance of the printed interconnects decreased under concave bending condition. However, at the same time, there is a rise in channel resistance which leads to the decrease in mobility. The trade-off between the two phenomena leads to the slight increase in the

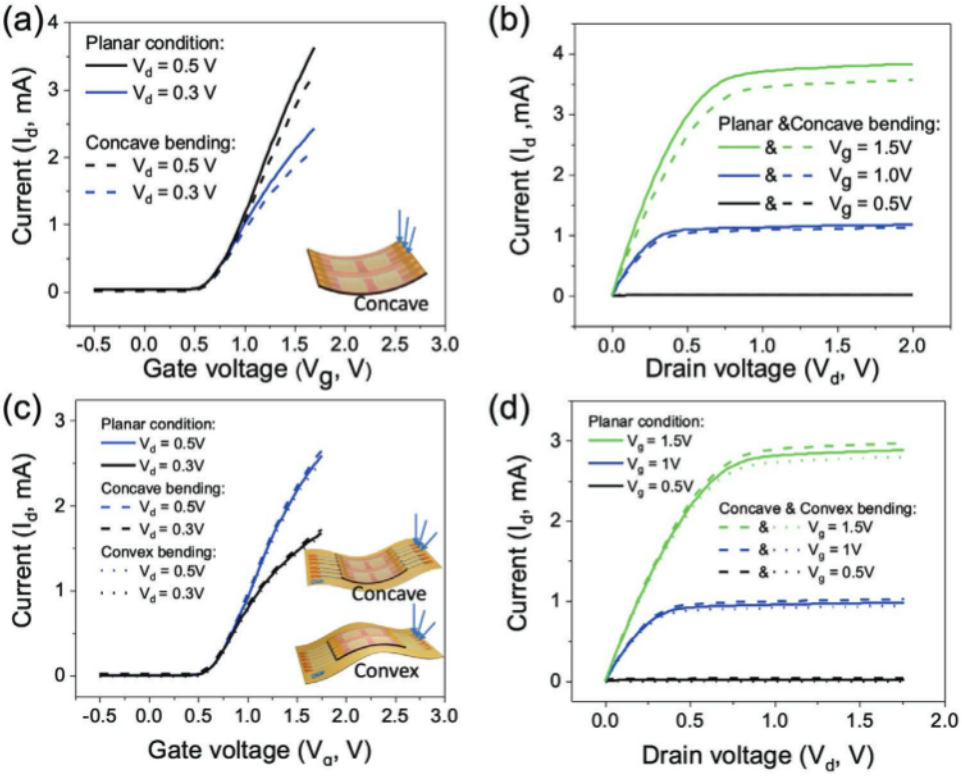

Figure 4. Device characterization after bonding by printing under planer and bending conditions for a,b) after thinning; c,d) after printing by bonding.

drain current under bending after printing interconnects. Nevertheless, such changes are negligible as we obtained similar carrier mobility ($\mu_{FE} \approx$ 630 $cm^2 V^{-1}s^{-1}$) and threshold voltage ($V_T = 0.6$ V) under planar and bending conditions after printing the interconnects.

4. Conclusion

We demonstrated a novel and cost-effective interconnect forming technology via non-contact printing. To elucidate the efficacy of the printing technology for interconnects, conductive tracks were realized to integrate the UTCs over flexible PCBs. Toward that, firstly, novel backside lapping, assisted with PMMA sacrificial technique, was used to reduce the MOSFET chip's thickness down to 34 ± 0.6 µm. Next, UTC was safely bonded using the high precision dispensing printing system, causing no damage to the thinned chip. This was confirmed by detailed electrical measurements of the MOSFETs after each process step, i.e., thinning, and bonding. The device showed similar transistor performance before and after chip thinning (780 $cm^2 V^{-1}s^{-1}$), confirming the effectiveness of the optimized thinning process. However, a slight degradation in device mobility (630 $cm^2 V^{-1}s^{-1}$) was observed after bonding which was attributed to the extra resistances added due to printed lines. Nevertheless, the mobility is still high enough for obtaining high-performance hybrid systems. Such minor performance degradation by printed lines can be prevented by using conductive pastes with lower resistivity. More research will be needed to this end. Finally, mechanical, and electrical robustness of both MOSFET and interconnects were tested under bending conditions (40 mm). The electrical measurements showed excellent stability for both interconnects and MOSFET devices. Thus, the presented approach shows good potential for realising hybrid systems on flexible foils with robust and cost-effective interconnects by printing.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available in the supplementary material of this article.

Keywords

heterogeneous integration, interconnects, non-contact printing, printed electronics, ultra-thin chips

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